What is claimed is:

1. A semiconductor device comprising:

a first impurity diffusion region formed in a semiconductor substrate;

a first insulating layer formed over the semiconductor substrate;

a capacitor formed over the first insulating layer and having a lower electrode, a ferroelectric layer, and an upper electrode;

an insulating capacitor protection layer made of material that is different from the first insulating layer, for covering an upper surface and a side surface of the capacitor;

a second insulating layer formed over the capacitor protection layer and the first insulating layer, and made of material that is etched selectively from the capacitor protection layer;

a first hole formed in the second insulating layer and positioned next to the side surface of the capacitor via the capacitor protection layer; and

a first conductive plug formed in the first hole and connected electrically to the first impurity diffusion region.

2. A semiconductor device according to claim 1, wherein two capacitors consisting of the capacitor are formed on both sides of the first hole via the capacitor protection layer respectively.

3. A semiconductor device according to claim 1, wherein the capacitor protection layer is formed of one of alumina, PZT material, and titanium oxide.

4. A semiconductor device according to claim 1, further comprising:

a second impurity diffusion region formed in the semiconductor substrate;

a second hole formed in the first insulating layer under the lower electrode of the capacitor and over the second impurity diffusion region; and

a second conductive plug formed in the second hole and connected electrically to the second impurity diffusion region.

5. A semiconductor device according to claim 4, wherein the second impurity diffusion region and the first impurity diffusion region constitute a part of a transistor that is formed on the semiconductor substrate.

6. A semiconductor device according to claim 1, wherein the capacitor protection layer is formed only on a surface of the capacitor.

7. A semiconductor device according to claim 1, wherein the capacitor protection layer is also extended between the first insulating layer and the second insulating layer around the capacitor.

8. A semiconductor device according to claim 7, wherein the capacitor protection layer is formed around the first hole.

9. A semiconductor device according to claim 1, wherein the capacitor protection layer has a plural-layered structure on the upper electrode of the capacitor.

10. A semiconductor device according to claim 1, wherein the first hole is extended into the first insulating layer.

11. A method of manufacturing a semiconductor device comprising the steps of:

forming a first impurity diffusion region in a semiconductor substrate;

forming a first insulating layer over the semiconductor substrate;

forming a first conductive layer, a ferroelectric layer, and a second conductive layer over the first insulating layer;

forming a capacitor by patterning the second conductive layer, the ferroelectric layer, and the first conductive layer using a first mask;

forming an insulating capacitor protection layer made of material, which is different from the first insulating layer, on an upper surface and side surfaces of the capacitor;

forming a second insulating layer made of material, that is etched selectively from the capacitor protection layer, over the capacitor protection layer and the first insulating layer;

forming a first hole, which comes into contact with

the capacitor protection layer on the side surface of the capacitor, in the second insulating layer; and

forming a first conductive plug, which is connected electrically to the first impurity diffusion region, in the first hole.

12. A method of manufacturing a semiconductor device according to claim 11, wherein the first hole is extended into the first insulating layer.

13. A method of manufacturing a semiconductor device according to claim 11, wherein two capacitors consisting of the capacitor are formed at an interval over the first impurity diffusion region, and

the first hole is formed between two capacitors in a self-alignment manner using the capacitor protection layers on upper surfaces and side surfaces of the capacitors.

14. A method of manufacturing a semiconductor device according to claim 13, wherein the first hole is formed by etching the second insulating layer through an opening portion of a second mask formed over the second insulating layer, and

the opening portion of the second mask has a diameter that is larger than an interval between two capacitors.

15. A method of manufacturing a semiconductor device according to claim 11, wherein the capacitor protection layer is formed by steps of forming a first

protection insulating layer on the second conductive layer, patterning the first protection insulating layer by using the first mask as well as the first conductive layer, the ferroelectric layer, and the second conductive layer, and forming a second protection insulating layer on the first protection insulating layer and the side surface of the capacitor.

16. A method of manufacturing a semiconductor device according to claim 15, further comprising the step of applying an anisotropic etching to the second protection insulating layer to remove the second protection insulating layer from an upper surface of the first insulating layer around the capacitor and leave the second protection insulating layer on the side surface of the capacitor.

17. A method of manufacturing a semiconductor device according to claim 11, further comprising the step of forming the first hole in the capacitor protection layer that extends from the capacitor onto the first insulating layer.

18. A method of manufacturing a semiconductor device according to claim 11, further comprising the steps of:

forming a second impurity diffusion region in the semiconductor substrate simultaneously with the first impurity diffusion region;

forming a second hole in the first insulating layer

under the lower electrode of the capacitor; and

forming a second conductive plug, which is connected electrically to the second impurity diffusion region, in the second hole.

19. A method of manufacturing a semiconductor device according to claim 18, further comprising the step of forming a gate electrode over the semiconductor substrate between the first impurity diffusion region and the second impurity diffusion region via a gate insulating layer.

20. A method of manufacturing a semiconductor device according to claim 11, wherein the step of forming the capacitor protection insulating layer is the step of forming one of alumina, PZT material, and titanium oxide.